AMENDMENTS TO THE CLAIMS

Please **CANCEL** claims 4 and 6 without prejudice to or disclaimer of the subject matter contained therein.

Please **AMEND** claims 1, 5 and 14 as shown below.

Please **ADD** claims 15-26 as shown below.

The following is a complete list of all claims in this application.

1. (Currently Amended) A liquid crystal display, comprising:

a liquid crystal panel including a plurality of gate lines, a plurality of data lines ~~perpendicularly intersecting the gate lines~~, a plurality of liquid crystal capacitors ~~coupled to a previous gate line and having liquid crystals between pixel electrodes and a common electrode~~, ~~and~~ a plurality of thin film transistors connected to ~~the pixel electrodes of~~ the liquid crystal capacitors, the gate lines and the data lines, and a plurality of storage capacitors, each storage capacitor connected between one of the liquid crystal capacitors and a previous gate line;

a timing controller receiving image signals and synchronization signals, and generating control signals;

a gate driver sequentially applying a stepped-wave pattern gate voltage to a plurality of the gate lines, the stepped-wave pattern gate voltage including a first interval for converting a ~~pixel~~ grayscale level of a first liquid crystal capacitor connected to a subsequent gate line through a first thin film transistor~~formed in a previous frame~~ to a first grayscale level, ~~and~~ a second interval for forming a path through which a data voltage of a second grayscale level is

~~applied~~transmitted to a second liquid crystal capacitor connected to a present gate line through a second thin film transistor by ~~controlling~~turning on the second thin film transistors ~~to on~~, and a third interval following the second interval and having the same polarity as a polarity of the data voltage; and

a data driver for applying ~~a~~the data voltage ~~of a second grayscale level supplied~~ to the second liquid crystal capacitors of the liquid crystal panel according to the control signals of the timing controller.

2. (Original) The liquid crystal display of claim 1, wherein the first grayscale level is a black grayscale level when in a normally white mode.

3. (Original) The liquid crystal display of claim 1, wherein the first grayscale level is a white grayscale level when in a normally black mode.

4. (Cancelled) ~~The liquid crystal display of claim 1, wherein the gate voltage further includes a third interval for applying a voltage of the same polarity as the data voltage during a predetermined interval before the first interval and following the turning off of the thin film transistors.~~

5. (Currently Amended) A drive method for a liquid crystal display, the liquid crystal display including: a liquid crystal panel having a plurality of gate lines, a plurality of data lines ~~perpendicularly intersecting the gate lines~~, a plurality of liquid crystal capacitors ~~coupled to a previous gate line and having liquid crystals between pixel electrodes and a common electrode~~,

~~and~~ a plurality of thin film transistors connected to ~~the pixel electrodes of~~ the liquid crystal capacitors, the gate lines, and the data lines, and a plurality of storage capacitors, each storage capacitor connected between one of the liquid crystal capacitors and a previous gate line; a gate driver for generating a signal supplied to gates of the thin film transistors; and a data driver for generating a data voltage supplied to the liquid crystal capacitors of the liquid crystal panel, the method comprising the steps of:

sequentially applying a stepped-wave pattern gate voltage to the gate lines, the stepped-wave pattern gate voltage including a first interval for converting a ~~pixel~~ grayscale level of a first liquid crystal capacitor connected to a subsequent gate line through a first thin film transistor~~formed in a previous frame~~ to a first grayscale level, ~~and~~ a second interval for forming a path through which a data voltage of a second grayscale level is ~~applied~~ transmitted to a second liquid crystal capacitor connected to a present gate line through a second thin film transistor by ~~controlling~~turning on the second thin film transistors ~~to on~~, and a third interval following the second interval and having the same polarity of the data voltage; and

applying the~~a~~ data voltage to the second liquid crystal capacitor of the liquid crystal panel.

6. (Cancelled) ~~The method of claim 5, wherein the gate voltage further includes a third interval for applying a voltage of the same polarity as the data voltage during a predetermined interval before the first interval and following the turning off of the thin film transistors.~~

7. (Original) The method of claim 6, wherein the gate voltage in the first interval is identical in polarity to a polarity of the gate voltage in the third interval.

8. (Original) The method of claim 6, wherein the gate voltage in the first interval is opposite in polarity to a polarity of the gate voltage in the third interval.

9. (Original) The method of claim 6, wherein the gate voltage in the third interval is $\pm$3V to $\pm$10V relative to a gate-off voltage.

10. (Original) The method of claim 6, wherein the third interval starts at a point where the second interval ends, and converts to a gate-off voltage at a position where the second interval doubles.

11. (Original) The method of claim 5, wherein the first grayscale level is a white grayscale level when in a normally black mode.

12. (Original) The method of claim 5, wherein the first grayscale level is a black grayscale level when in a normally white mode.

13. (Original) The method of claim 5, wherein the gate voltage in the first interval is $\pm$3V to $\pm$10V relative to a gate-off voltage.

14. (Currently Amended) The method of claim 5, wherein a starting point of the first interval is within about 0.5~~μms~~ to~~–~~ about 5~~μms~~ from a starting point of the second interval.

15. (New) A liquid crystal display, comprising:

first and second gate lines sequentially supplied with a gate signal;

a data line transmitting a first data voltage and a second data voltage;

a first switching element connected to the first gate line and the data line and selectively transmitting the first data voltage;

a second switching element connected to the second gate line and the data line and selectively transmitting the second data voltage;

a first liquid crystal capacitor connected to the first switching element;

a second liquid crystal capacitor connected to the second switching element;

a storage capacitor connected between the second liquid crystal capacitor and the first gate line;

a data driver applying the first and the second data voltages to the data line; and

a gate driver sequentially applying the gate signal to the first and the second gate lines,

wherein the gate signal has first to fourth voltages during sequentially arranged first to fourth time intervals, respectively.

16. (New) The liquid crystal display of claim 15, wherein the first switching element and the second switching element turn on by the second voltage and turn off by the fourth voltage.

17. (New) The liquid crystal display of claim 16, wherein the first liquid crystal capacitor and the second liquid crystal capacitor are supplied with a common voltage, the third voltage of the gate signal applied to the first gate line is higher than the fourth voltage when the first data voltage is higher than the common voltage, and the third voltage of the gate signal

applied to the first gate line is lower than the fourth voltage when the first data voltage is lower than the common voltage.

18. (New) The liquid crystal display of claim 17, wherein both the first and the third voltages are higher or lower than the fourth voltage.

19. (New) The liquid crystal display of claim 18, wherein the liquid crystal display operates in normally white mode.

20. (New) The liquid crystal display of claim 17, wherein one of the first and the third voltages is higher than the fourth voltage and the other of the first and the third voltages is lower than the fourth voltage.

21. (New) The liquid crystal display of claim 20, wherein the liquid crystal display operates in normally black mode.

22. (New) The liquid crystal display of claim 16, wherein both the first and the third voltages are higher or lower than the fourth voltage.

23. (New) The liquid crystal display of claim 22, wherein the third voltage has a value between the first voltage and the fourth voltage.

24. (New) The liquid crystal display of claim 16, wherein one of the first and the third voltages is higher than the fourth voltage and the other of the first and the third voltages is lower than the fourth voltage.

25. (New) A liquid crystal display, comprising:

first and second gate lines sequentially supplied with a gate signal;

a data line transmitting a first data voltage and a second data voltage;

a first switching element connected to the first gate line and the data line and selectively transmitting the first data voltage;

a second switching element connected to the second gate line and the data line and selectively transmitting the second data voltage;

a first liquid crystal capacitor connected between the first switching element and a common voltage;

a second liquid crystal capacitor connected between the second switching element and the common voltage;

a storage capacitor connected between the second liquid crystal capacitor and the first gate line;

a data driver applying the first and the second data voltages to the data line; and

a gate driver sequentially applying the gate signal to the first and the second gate lines,

wherein the gate signal has first, second, and third voltages during first, second, and third time intervals, respectively, and the first and the second switching elements turn on by the first voltage and turn off by the second voltage, the third interval precedes the first time interval, and a polarity of the third voltage with respect to the second voltage is the same as a polarity of the data voltage with respect to the common voltage.

26. (New) The liquid crystal display of claim 25, wherein the gate signal further has a fourth voltage, which has a polarity with respect to the second voltage equal to the polarity of the data voltage, during a fourth time interval following the first time interval.